SBC8233

386SX All-in-One
Half-size
CPU Card Series
with CRT/LCD

User's Manual

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ESD Precautions

Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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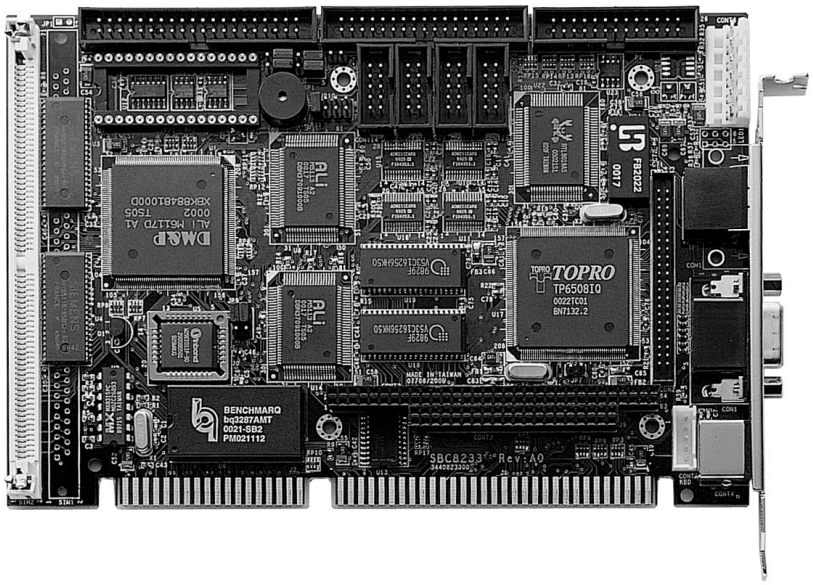
Chapter 1
Introduction

1.1 General Description



The **SBC8233 Series** contains all standard motherboard features such as 386SX-40 compatible CPU, CRT and Flat Panel controller, serial and parallel ports, floppy, and EIDE disk controller.

The SSD socket can accommodate a DiskOnChip® 2000, a new generation of high performance single chip Flash Disks.

The **SBC8233 Series** is for basic control applications in demanding embedded applications. Since the card implements all key functions of a full PC/AT compatible system any standard PC compiler or debugger can be used, resulting in a significantly reduced software development cycle.

1.2 Specifications

- **Embedded CPU:** ALi M6117D is an implementation of an INTEL compatible 386SX-40 CPU, realtime clock, a watchdog timer and ALi's M1217B chipset
- **BIOS:** Y2K compliant AMI system BIOS
- **Onboard Memory:** 4MB EDO RAM (Bank0)
- **DRAM Memory:** 1 x 72-pin SIMM socket (single side type) supporting up to 16MB EDO RAM
- **Bus Interface:** ISA and PC/104
- **Data Bus:** 16-bit
- **Bus Speed:** PC/104 - 8 MHz
  (Above values are defaults, bus speeds are programmable up to 16MHz)
- **DMA Channels:** 7
- **Interrupt Levels:** 15
- **Enhanced IDE:** supports one port and up to two enhanced IDE (AT Bus) hard drives
- **Watchdog Timer:** generates a RESET, NMI or an IRQ when your application loses control over the system. Optionally the watchdog can trigger a user-specified interrupt. The watchdog is configurable from 30.5µs to 512 seconds (in 30.5µs segments)
- **Real-time Clock:** included in M6117D with onboard lithium battery backup for 10 years of data retention. CMOS data backup of BIOS setup and BIOS default.
- **Keyboard / Mouse Connectors:** supports different type connectors of AT Keyboard and PS/2-mouse

1.2.1 High Speed Multi I/O

- **Chipset:** ALi 5113
- **Serial ports:** supports high speed RS-232 port, high speed RS-232/485 port (jumper selectable). Both with 16C550 UART and 16 byte FIFO
- **FDD Interface:** supports up to two floppy drives, 5¼" (360 KB or 1.2 MB) and 3½" (720 KB, 1.44 MB)
- **Bi-directional Parallel Port:** supports SPP, EPP and ECP mode

1.2.2 Environmental and Power

- **Power Requirements:** Single voltage +5 V
- **Board Dimensions:** 185 (L) x 122 (W) mm.
- **Board Weight:** 240 g
- **Extended Operating Temperature:** 0~+60 °C

1.3 VGA Interface

- **Chipset:** TOPRO TP6508IQ
- **Memory:** 1 MB onboard
- **System Bus:** 16-bit ISA bus
- **Panel Data Bus:** 24-bit
- **Display:** CRT and Flat Panel Mono/TFT/DSTN/EL

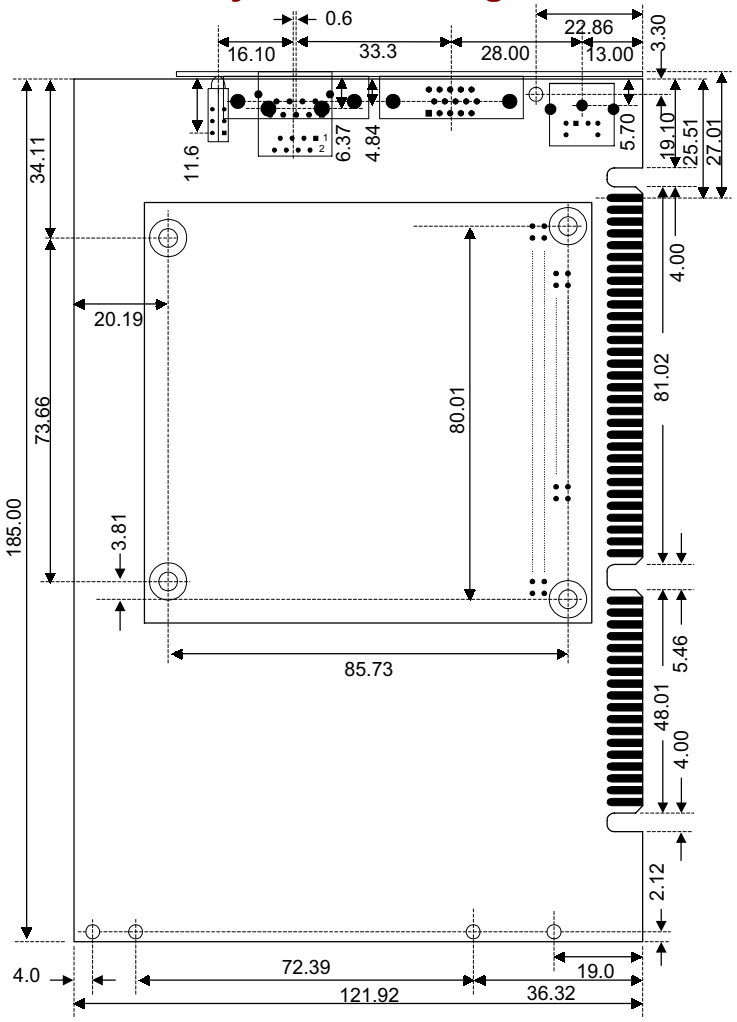
1.4 DiskOnChip® Flash Disk

1.4.1 Flash Disk DiskOnChip®

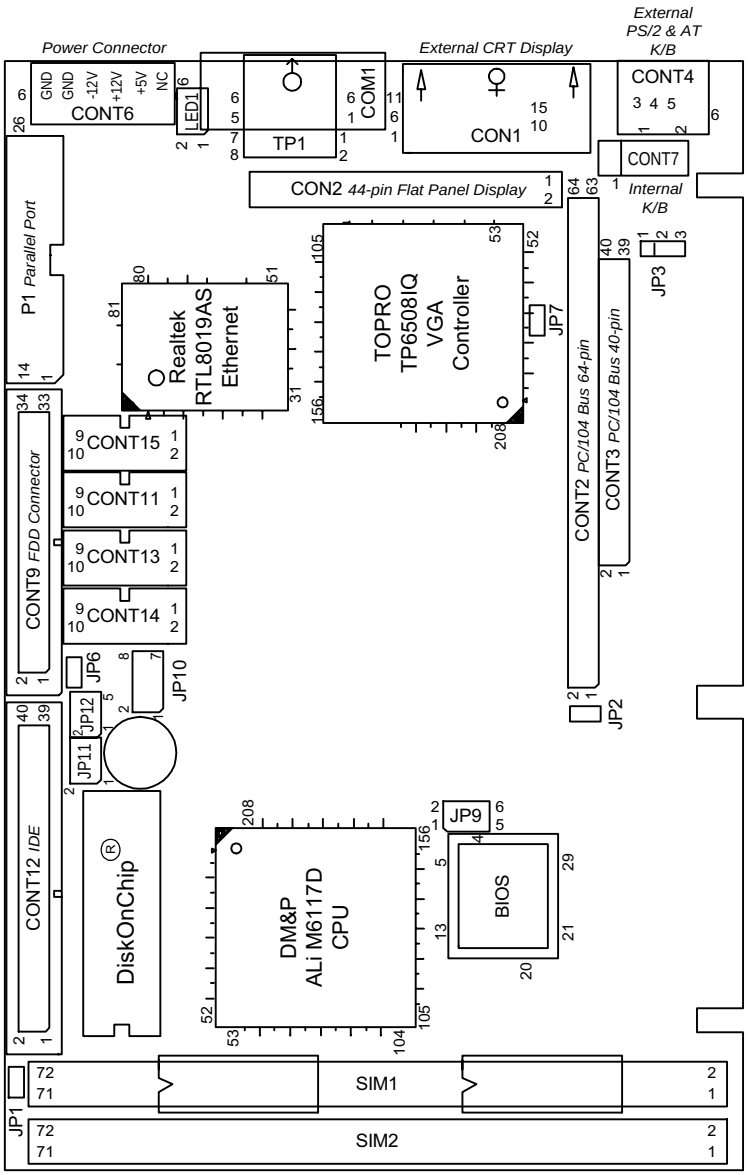
- **Package:** Single Chip Flash Disk in 32-pin DIP JEDEC
- **Capacity:** Up to the most updated capacity
- **Data Reliability:** ECC/EDC error correction
- **Memory Window:** 8 Kbyte

Chapter 2
Installation

2.1 Board Layout and Fixing Holes



2.2 Placement



2.3 Jumper Settings

Making the proper jumper settings configures the **SBC8233 Series** to match the needs of your application. The following table shows the default jumper settings onboard **SBC8233 Series**.

Jumper	Function	Default
JP1	Reset Jumper: Normal	Open
JP2	Clear CMOS Setting: Normal	Open
JP7	VGA IRQ9 Operation: w/o IRQ9	Open
JP9	IRQ3/4/10/11 selection for COM3: IRQ10	Short 3-5
	IRQ3/4/10/11 selection for COM4: IRQ11	Short 4-6
JP10	RS-232/422/485 selection for COM2: RS-232	Short 1-2
JP11	RS-232/422/485 for COM2 mode: RS-232	Short 3-5, 4-6
JP12	RS-232/422/485 for COM2 mode: RS-232	Short 3-5, 4-6

2.3.1 Reset Jumper: JP1

Options	Settings
Reset	Short 1-2
Normal	Open (default)

2.3.2 Clear CMOS Setting: JP2

Options	Settings
Clear CMOS	Short 1-2
Normal	Open (default)

2.3.3 VGA IRQ9 Operation: JP7

Options	Settings
VGA Operation w/o IRQ9	Open (default)
VGA Operation w/ IRQ9	Short

2.3.4 IRQ3/4/10/11 selection for COM3/COM4: JP9

Mode	IRQ3	IRQ4	IRQ10	IRQ11
COM3	Short 1-3	Open	Short 3-5 (default)	Open
COM4	Open	Short 2-4	Open	Short 4-6 (default)

2.3.5 COM2 RS-232/422/485 Setting: JP10

COM2 Mode	Settings
RS-232	Short 1-2 (CONT11 active) - default
RS-422	Short 3-4
RS-485	Short 5-6

2.3.6 RS232/422/485 Selection for COM2 Mode: JP11, JP12

Options	JP11	JP12
RS232	Short 3-5, 4-6 (default)	Short 3-5, 4-6 (default)
RS-422/485	Short 1-3, 2-4	Short 1-3, 2-4

2.4 Connectors

Connectors allow the CPU card to connect with other parts of the system. Some problems encountered by the system may be a result of loose or improper connections. Ensure that all connectors are in place and firmly attached. The following table lists the function of all connectors on the **SBC8233 Series**. Their corresponding pin assignments are described in Chapter 3.

Label	Connector	Label	Connector
CON1	External female 15-pin D-type CRT Display	**CONT12**	IDE
CON2	Internal 44-pin Flat Panel Display	**CONT13**	Internal 10-pin box header connector for COM3
CONT2	PC/104 bus 64-pin	**CONT14**	Internal 10-pin box header connector for COM4
CONT3	PC/104 bus 40-pin	**CONT15**	Internal 10-pin box header connector for COM1
CONT4	External PS/2 and AT keyboard	**JP3**	Power LED
CONT6	Power	**JP6**	IDE LED
CONT7	Internal AT-keyboard	**P1**	Parallel Port
CONT9	FDD	**SIM1**	Memory bank 0 (EDO DRAM)
COM1	External 9-pin male D-type connector for COM1	**SIM2**	Memory bank 1 (EDO DRAM)
CONT11	Internal 10-pin box header connector for COM2	**TP1**	Ethernet RJ-45 connector

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Chapter 3
Hardware Description

3.1 Microprocessors

The **SBC8233 Series** supports an onboard DM&P ALi M6117D microprocessor. Systems based on these CPUs can be operated under UNIX, OS/2, Windows 95 and MS-DOS environments.

3.2 BIOS

System BIOS used on the **SBC8233 Series** is AMI Plug and Play BIOS. The **SBC8233 Series** contains a single Flash EPROM and supports power-on modification of the system BIOS. Refer to Chapter 5 for a detailed description of the AMI BIOS software utility program.

3.3 System Memory

The **SBC8233 Series** supports one 72-pin SIMM socket (Bank 1) plus 4MB onboard (Bank 0). With the additional maximum memory capactiy of Bank 1 (16MB), the **SBC8233 Series** supports a total system memory of 20MB. The memory module can come in sizes of 256K, 512K, 1MB, 4MB, 8MB, and 16MB EDO DRAMs.

3.4 Interrupt Controller

The **SBC8233 Series** is a 100% PC compatible control board. It consists of 16 ISA interrupt request lines. The mapping list of the 16 interrupt request lines is shown on the following table.

NMI	Parity check error
IRQ0	System timer output
IRQ1	Keyboard
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port #2
IRQ4	Serial port #1
IRQ5	Parallel port #2
IRQ6	Floppy disk controller
IRQ7	Parallel port #1
IRQ8	Real time clock
IRQ9	Reserved
IRQ10	Serial port #3
IRQ11	Serial port #4
IRQ12	PS/2 Mouse
IRQ13	Math coprocessor
IRQ14	Primary IDE channel
IRQ15	Secondary IDE Channel

3.5 IDE Interface Connector

The **SBC8233 Series'** built-in ISA bus enhanced IDE controller provides enhanced IDE interface supporting PIO mode 4. IDE connector of **SBC8233 Series** features one standard 40-pin header connector (**CONT12**).

CONT12: 40-pin IDE Connector Pin Assignment

Pin	Description	Pin	Description	Pin	Description
1	Reset #	2	GND	3	Data 7
4	Data 8	5	Data 6	6	Data 9
7	Data 5	8	Data 10	9	Data 4
10	Data 11	11	Data 3	12	Data 12
13	Data 2	14	Data 13	15	Data 1
16	Data 14	17	Data 0	18	Data 15
19	GND	20	No connector	21	No connector
22	GND	23	IOW #	24	GND
25	IOR #	26	GND	27	No connector
28	No connector	29	No connector	30	GND-Default
31	Interrupt IRQ14	32	IOCS16	33	SA1
34	No connector	35	SA0	36	SA2
37	HDC CS0 #	38	HDC CSI #	39	HDD Active #
40	GND				

3.6 Display Interface

The **SBC8233 Series** has an onboard VGA interface. The specifications and features are described as follows:

3.6.1 Chipset

The **SBC8233 Series** uses a TOPRO TP6508IQ for its SVGA controller, which supports conventional analog CRT monitor or flat panel. In addition, it also supports interlaced and non-interlaced analog monitors (color and monochrome VGA) in high-resolution modes while maintaining complete IBM VGA compatibility. Multiple frequency (multisync) monitors are handled as if they were analog monitors.

3.6.2 Display Memory

With 1 MB memory, the VGA controller can drive CRT displays or color panel displays with resolutions up to 1024 x 768 at 256 colors.

3.6.3 VGA/Flat Panel Connectors

The **SBC8233 Series** has two connectors that support CRT VGA and flat panel displays, individually or simultaneously. **CON1** is a 15-pin D-type connector commonly used for the CRT VGA display, and **CON2** is a 44-pin connector for flat panel connection. Configuration of the VGA interface is done via the software utility and no jumper setting is required.

CON1: CRT/VGA Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal
1	Red	2	Green	11	No connector
3	Blue	4	No connector	12	No connector
5	GND	6	GND	13	HSYNC
7	GND	8	GND	14	VSYNC
9	No connector	10	GND	15	No connector

CON2: 44-pin Connector for Flat Panel

Pin	Description	Pin	Description	Pin	Description
1	12V	2	12V	3	GND
4	GND	5	VDDM	6	VDDM
7	FPVEE	8	GND	9	PO
10	P1	11	P2	12	P3
13	P4	14	P5	15	P6
16	P7	17	P8	18	P9
19	P10	20	P11	21	P12
22	P13	23	P14	24	P15
25	P16	26	P17	27	P18
28	P19	29	P20	30	P21
31	P22	32	P23	33	GND
34	GND	35	SCLK	36	FLM
37	M	38	LP	39	GND
40	ENABKL	41	GND	42	ASHFCLK
43	VDDM	44	VDDM		

3.6.4 Flat Panel Connector Pin Description

Name	Description
P0~P35	Flat panel data output
ENABKL	Activity Indicator and Enable Backlight outputs
SHFCLK	Shift clock. Pixel clock for flat panel data
M	M signal for panel AC drive control
LP	Latch pulse. Flat panel equivalent of HSYNC
FLM	First line marker. Flat panel equivalent of VSYNC
+12VM	+12V power controlled by chipset
ENAVEE	Power sequencing controls for panel LCD bias volt
VDDM	5V

3.7 Floppy Disk Controller

The **SBC8233 Series** provides a 34-pin connector, **CONT9**, for support of a single floppy drive. The floppy drive could be any one of the following types: 3.5" 720KB or 1.44MB/2.88MB.

CONT9: FDD Connector Pin Assignment

Pin No.	Signal	Pin No.	Signal
1-33 (odd)	GND	20	Step Pulse
2	High Density	22	Write Data
4, 6	Unused	24	Write Enable
8	Index	26	Track 0
10	Motor Enable A	28	Write Protect
12	Driver Select B	30	Read Data
14	Driver Select A	32	Select Head
16	Motor Enable B	34	Disk Change
18	Direction		

3.8 Parallel Port Interface

The **SBC8233 Series** has one bidirectional parallel port (**P1**) that supports SPP, EPP, or ECP modes.

- **Standard mode:** IBM PC/XT, PC/AT and PS/2™ compatible with bi-directional parallel port
- **Enhanced mode:** Enhance parallel port (EPP) compatible with EPP 1.7 and EPP 1.9 (IEEE 1284 compliant)
- **High speed mode:** Microsoft and Hewlett Packard extended capabilities port (ECP) IEEE 1284 compliant

The address selection of the onboard parallel port, in LPT1 (378H), LPT2 (278H), or disabled, is configured within the BIOS CMOS setup utility.

Pin	Description	Pin	Description
1	Strobe	2	Data 0
3	Data 1	4	Data 2
5	Data 3	6	Data 4
7	Data 5	8	Data 6
9	Data 7	10	Acknowledge #
11	Busy	12	Paper Empty #
13	Printer Select	14	Auto Form Feed #
15	Error #	16	Initialize #
17	Printer Select In #	18	GND
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	GND	26	No connector

3.9 Serial Port Interface

The **SBC8233 Series** has four onboard serial ports, **COM1 (CONT15)**, **COM3 (CONT13)** and **COM4 (CONT14)** are RS-232 and **COM2 (CONT11)** is RS-232/422/485, jumper selectable. All four ports feature +5V/12V power capability on pin 1 and pin 8, depending on the jumper setting.

3.9.1 Serial Ports IRQ Selection

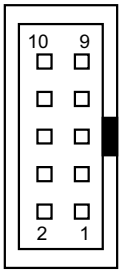
The **SBC8233 Series** has four onboard serial ports, with **COM1**, **COM3**, and **COM4** as RS-232 and **COM2** as RS-232/422/485, both selected via jumper setting. All ports have +5V/12V power capability on both pin 1 and pin 8 or pin 9 depending on jumper selection.

3.9.2 Serial Ports +5V and +12V Power Selection

The four COM ports have +5V/+12V power capability on pin 1 and pin 8, depending on the jumper setting. The RS-232 pin assignments are listed below.

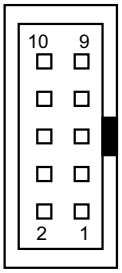
CONT11/13/14/15: COM2/3/4/1 Serial Port Connectors Pin Assignment

Pin	Description	Pin	Description
1	Data Carrier Detect (DCD)	2	Data Set Ready (DSR)
3	Receive Data (RXD)	4	Request to Send (RTS)
5	Transmit Data (TXD)	6	Clear to Send (CTS)
7	Data Terminal Ready (DTR)	8	Ring Indicator (RI)
9	Ground (GND)	10	Ground (GND)



The RS-422/485 pin assignments for **CONT11** (COM2) are listed on the following table.

CONT11 Pin	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	DSR	No connector	No connector
3	RX	TX+	DATA+
4	RTS	No connector	No connector
5	TX	RX+	No connector
6	CTS	No connector	No connector
7	DTR	RX-	No connector
8	RI	No connector	No connector
9	GND	GND	GND
10	GND	GND	GND



3.10 DiskOnChip®

3.10.1 Setup a DiskOnChip® Flash Disk

Installation Instructions

1. Make sure the power of **SBC8233 Series** is OFF.
2. Plug the DiskOnChip® device(s) into its socket. Verify the direction is correct (pin 1 of the DiskOnChip® is aligned with pin 1 of the socket)
3. Set address for both DiskOnChip® devices (note that the last two settings are for normal EPROM or Flash devices)
4. Power up the system
5. During power up you may observe the messages displayed by the DiskOnChip® when its drivers are automatically loaded into system's memory
6. At this stage the DiskOnChip® can be accessed as any disk in the system
7. If the DiskOnChip® is the only disk in the system, it will appear as the first disk (drive C: in DOS)
8. If there are more disks besides the DiskOnChip®, the DiskOnChip® will appear by default as the last drive, unless it was programmed as first drive. (Please refer to the DiskOnChip® utilities user manual).

9. If you want the DiskOnChip® to be bootable:
   a. Copy the operating system files into the DiskOnChip® by using the standard DOS command (for example: sys d:).
   b. The DiskOnChip® should be the only disk in the systems or should be configured as the first disk in the system (c:) using the DUPDATE utility.

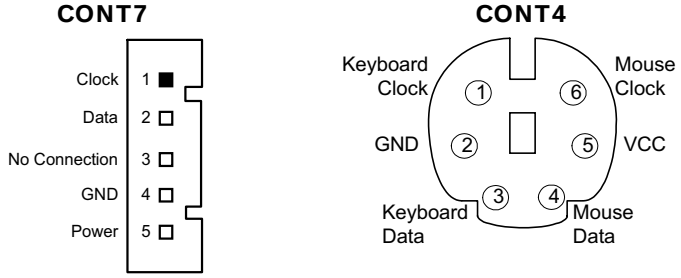
For more information on DiskOnChip® technology, visit M-Systems Web site **http://** www.m-sys.com where you can find Utilities Manual, Data Sheets and Application Notes. In addition, you can find the lasted DiskOnChip® S/W Utilities.

3.11 Real Time Clock and CMOS RAM

The **SBC8233 Series** contains a M6117D Real Time Clock (RTC). The CMOS RAM stores the system configuration information entered via the SETUP program. A battery, with power lasting 10 years, keeps the stored information on the RTC and CMOS RAM active when system power is turned off.

3.12 Keyboard and PS/2 Mouse Connector

The **SBC8233 Series** provides an external AT keyboard and PS/2 mouse interface via a DIN connector (**CONT4**), and an internal AT keyboard interface via a 5-pin connector (**CONT7**).

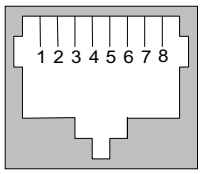


3.13 Ethernet Connector

The RJ-45 provides a RJ-45 interface via **TP1**. To connect the **SBC8233 Series** to a 10-Base-T or 100-Base-T hub, just plug one end of the cable into the **TP1** and connect the other end (phone jack) of the cable to a 10/100-Base-T hub.

TP1: RJ-45 Connector Pin Assignment

Pin	Signal
1	Tx+ (Data transmission positive)
2	Tx- (Data transmission negative)
3	Rx+(Data reception positive)
6	Rx- (Data reception negative)
other	Not use



RJ-45

3.14 PC/104 Connectors

The PC/104 is an industrial standard. It is a compact form factor with dimensions of 3.6” x 3.8” and is fully compatible with the ISA Bus. The PC/104 interface is able to adapt the off-the-shelf PC/104 modules, such as sound module, fax modem module and multi-I/O module…etc.

CONT2: PC/104 Bus Pin Assignment

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	IOCHCHK*	2	GND	3	SD7	4	RESETDRV
5	SD6	6	+5V	7	SD5	8	IRQ9
9	SD4	10	-5V	11	SD3	12	DRQ2
13	SD2	14	-12V	15	SD1	16	ENDXFR*
17	SD0	18	+12V	19	IOCHRDY	20	GND
21	AEN	22	SMEMW*	23	SA19	24	SMEMR*
25	SA18	26	IOW*	27	SA17	28	IOR *
29	SA16	30	DACK3*	31	SA15	32	DRQ3
33	SA14	34	DACK1*	35	SA13	36	DRQ1
37	SA12	38	REFRESH*	39	SA11	40	SYSCLK

Continued . . . . .

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
41	SA10	42	IRQ7	43	SA9	44	IRQ6

45	SA8	46	IRQ5	47	SA7	48	IRQ4
49	SA6	50	IRQ3	51	SA5	52	DACK2*
53	SA4	54	TC	55	SA3	56	SALE
57	SA2	58	+5V	59	SA1	60	OSC
61	SA0	62	GND	63	GND	64	GND

CONT3: PC/104 Bus Pin Assignments

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	GND	2	GND	3	MEMCS16*	4	SBHE*
5	IOCS16*	6	LA23	7	IRQ10	8	LA22
9	IRQ11	10	LA21	11	IRQ12	12	LA20
13	IRQ15	14	LA19	15	IRQ14	16	LA18
17	DACK0*	18	LA17	19	DRQ0	20	MEMR*
21	DACK5*	22	MEMW*	23	DRQ5	24	SD8
25	DACK6*	26	SD9	27	DRQ6	28	SD10
29	DACK7*	30	SD11	31	DRQ7	32	SD12
33	+5V	34	SD13	35	MASTER*	36	SD14
37	GND	38	SD15	39	GND	40	(KEY)

3.15 Pin Assignments of Other Connectors

CONT6: Power Connector

Pin	Description	Pin	Description
1	No connector	4	-12V
2	+5V	5	GND
3	+12V	6	GND

JP3: Power LED

Pin	Description
1	Vcc
2	No connector
3	Ground

JP6: IDE LED

Pin	Description
1	Vcc
2	Signal

Chapter 4
Ethernet

4.1 Introduction

The **SBC8233 Series** is equipped with a high performance Plug and Play Ethernet interface which is fully compliant with the IEEE 802.3 standard, and consisting of a RJ-45 interface.

The RTL8019AS integrates the RTL8019 and 16K-byte SRAM in a single chip. It is designed not only to provide more friendly functions but also to save the effort of SRAM sourcing and inventory.

4.2 Features

- RTL8019 software compatible
- Supports PnP auto detect mode
- 16k byte SRAM built in
- Supports flash memory read/write
- Supports UTP and auto-detect
- Supports IO address fully decode mode
- Makes PnP jumper option more user-friendly
- Improves the blinking problem of CRS LED when the cable is not connected

4.3 Drivers Supported

Bundled with popular software drivers, the **SBC8233 Series** Ethernet interface allows great flexibility to work with all major networking operating systems including Novell NetWare v2.x, v3.x, Microsoft LAN Manager, Win3.1, Win95, IBM LAN Server, SCO UNIX or other ODI, NDIS and Packet drive compliant operating systems.

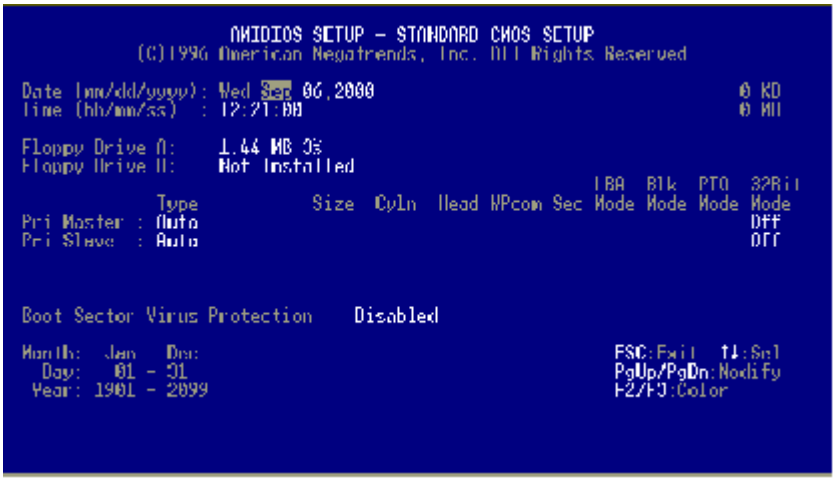
Chapter 5
AMI BIOS Setup

When the system is powered on, the BIOS will perform diagnostics and initialize system components, including the video system. (This is self-evident when the screen first flicks before the Video Card header is displayed). This is commonly referred as POST (Power-On Self Test). Afterwards, the computer will proceed its final boot-up stage by calling the operating system. Just before that, the user may interrupt to have access to SETUP.

Pressing the <DEL> key after resetting (CTRL-ALT-DEL) or powering up the computer enters the AMI BIOS. You can bypass the extended CMOS settings by holding the <INS> key down during boot-up. This is really helpful, especially if you bend the CMOS settings right out of shape and the computer won't boot properly anymore. The following pages are meant to give you a better insight into the options you have to setup your system. Many options depend on the choice of type of memory, memory speed, peripherals and the programs that you will be running. The effect on many of these settings is related to system performance that can destabilize operation. We urge you to proceed with caution.

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

5.1 Standard CMOS Setup


AMIBIOS SETUP - STANDARD CMOS SETUP
(C)1996 American Megatrends, Inc. All Rights Reserved
Date (mm/dd/yyyy): Wed Sep 06,2000
Time (hh/mm/ss) : 12:21:00
Floppy Drive A: 1.44 MB 3½
Floppy Drive B: Not Installed
Type Size Cyln Head WPcom Sec LBA Mode Blk Mode PIO Mode 32Bit Mode
Pri Master : Auto Off
Pri Slave : Auto Off
Boot Sector Virus Protection Disabled
Month: Jan - Dec
Day: 01 - 31
Year: 1901 - 2099
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F2/F3:Color

- **Date**
  The BIOS determines the day of the week from the other date information; this field is for information only.

- **Time**
  The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field . Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

- **Floppy Drive A, B**
  Select the correct specifications for the diskette drive(s) installed in the computer.

None	No diskette drive installed
360K	5.25 in5-1/4 inch PC-type standard drive
1.2M	5.25 in5-1/4 inch AT-type high-density drive
720K	3.5 in3-1/2 inch double-sided drive
1.44M	3.5 in3-1/2 inch double-sided drive

- **Hard Disks**
  The BIOS supports up to four IDE drives. This section does not show information about other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

NOTE: *It is recommended that you select type AUTO for all drives.*

The BIOS can automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots. If you do not want to select drive type AUTO, other methods of selecting the drive type are available:

1. Match the specifications of your installed IDE hard drive(s) with the preprogrammed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the IDE HDD AUTO DETECTION function in Setup.

Here is a brief explanation of drive specifications:

Type: The BIOS contains a table of predefined drive types. Each defined drive type has a specified number of cylinders, number of heads, write precompensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any predefined type are classified as type USER.

Size: Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.

Cyln: Number of cylinders

Head: Number of heads

WPcom: Write Precompensation. Older HDD's have the same number of sectors per track at the innermost tracks as at the outermost tracks. This means that the data density at the innermost tracks is higher and thus the bits are lying closer together. Areas having the same direction tend to float away from each other and areas having opposite direction tend to float towards each other making the data less reliable after some time. To avoid this, starting from the WP cylinder, bits are written on the surface making your data last longer. Starting with this Cylnumber until the end of Cylnumber the writing starts earlier on the disk. In modern HDs (all ATBUS and SCSI, Small Computer Systems Interface) this entry is useless.

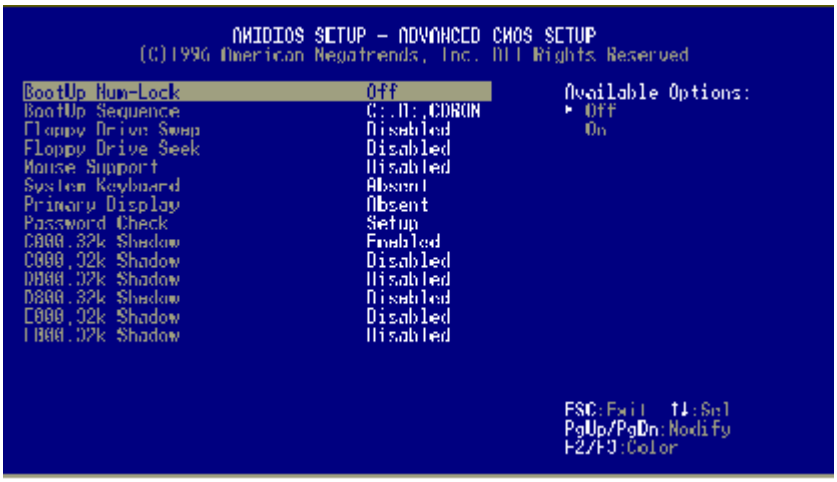
Sec: Number of sectors

LBA Mode	Logical Block Addressing Mode enables support for IDE drives with capacities greater than 528 MB (On/Off)
Block Mode	Support IDE drives that use Block Mode. (On/Off)
32Bit Mode	Support IDE drives that permit 32-bit accesses. (On/Off)

PIO Mode IDE Programmed I/O mode. PIO programming also works with ATAPI CD-ROM drives. The settings are Auto, 0, 1, 2, 3, 4, or 5. Click on Auto to allow AMIBIOS to automatically find the PIO mode that the IDE drive being configured uses. If you select 0-5 you must make absolutely certain that you are selecting the PIO mode supported by the IDE drive being configured.

- **BootSector Virus Protection**
  It is not exactly a virus protection. All it does is whenever your boot sector is accessed for writing, it gives a warning to the screen allowing you to disable the access or to continue. Extremely annoying if you use something like OS/2 Boot Manager that needs to write to it. It is completely useless for SCSI or ESDI (Enhanced Small Device Interface) drives as they use their own BIOS on the controller. Disabled recommended. If you want virus protection, use a TSR (Terminate and Stay Resident) virus detection (Norton, Central Point, etc...). Scan by McAfee is also a good idea. Available on most FTP servers, it is shareware.

5.2 Advanced CMOS Setup



- **1st Boot Device**
  Specifies the first device for which to look and use for booting the system. Options are : Disabled 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD, ATAPI CDROM, SCSI or NETWORK. ARMD (FDD/HDD) means “ATAPI Removable Media Device”.

- **2nd Boot Device**
  Specifies the second device for which to look and use for booting the system. Options are : Disabled 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD, ATAPI CDROM, SCSI or NETWORK.

- **Floppy Drive Swap**
  This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

- **PS/2 Mouse Support**
  This setting is specially for those users who whish to connect a PS/2 mouse. Enabling reserves IRQ 12 for the PS/2 mouse. Disabling releases the IRQ 12 for use by another system component.

- **System Keyboard**
  “Present”. If “Absent” is selected this option sets the BIOS to pass the keyboard test in the POST, allowing to reset a PC without a keyboard (file server, printer server, etc.), without the BIOS producing a keyboard error.

- **Primary display**
  The type of display standard you are using. The most frequent is VGA/PGA/EGA. Modern computers have VGA (Video Graphics Array). If you have an older black/ white display select Mono. If you want to use the board without display controller set this value to “Absent”. This option sets the BIOS to pass the display controller test in the POST, allowing to boot a PC without a display controller. Even if set to “Absent” the board will still try to initialize a display card if present.

- **Password Check**
  If you have set a password, select whether the password is required every time the System boots, or only when you enter the BIOS Setup.

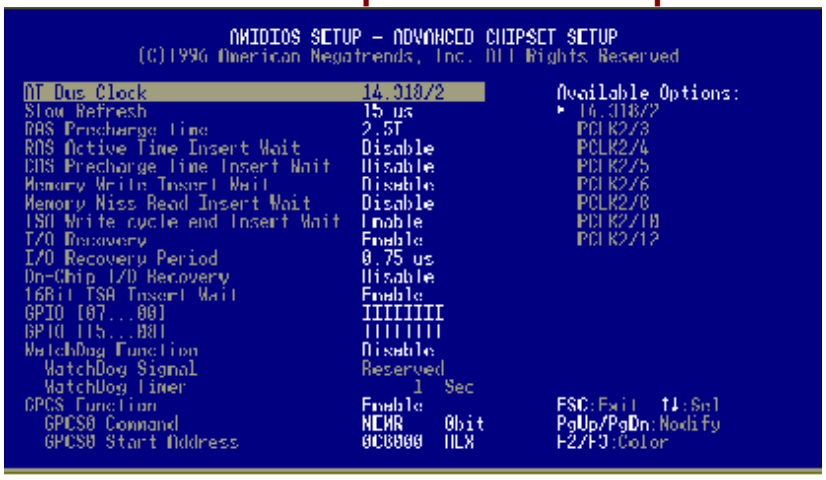
Always	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

- **C8000, 16 K Shadow**
  Specifies whether the specified area of ROM is to be shadowed and if shadowed, whether it should be written to or read from cache memory. The fail-safe default is Disabled.

  CAUTION: *Some option ROMs do not operate properly when shadowed.*

  - CC000, 16 K Shadow
  - D0000, 16 K Shadow
  - D4000, 16 K Shadow
  - D8000, 16 K Shadow
  - DC000, 16 K Shadow

5.3 Advanced Chipset CMOS Setup



- **VGA Frame Buffer Size**
  The STPC implements a single memory subsystem for both the system as well as the frame buffer memory. In other words, the size of the DRAM available to the system is reduced by the size of the DRAM allocated to the frame buffer. The lower range of the DRAM, starting from the DRAM address 00h, is allocated to frame buffer. The rest of the memory is used by the system.

- **ISACLK**
  Set the speed of the ISA bus here. The settings are tied to the speed of the PCI bus. If the PCI bus operates at 33 MHz, a setting of PCICLK/4 (default) would yield an ISA bus speed of approximately 8 MHz, the standard speed of the ISA bus. While most devices operate at higher ISA bus speeds, try a slower bus speed if your ISA device does not function properly.

- **Memory Hole**
  You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
  The memory hole can be configured as 1 MB (15-14MB), 2 MB (15-13MB), 4 MB (15-11MB), 8 MB (15-7MB) or disabled.

5.4 Peripheral Setup

- **Onboard FDC**
  Enable/disable or Auto detect FDD Controller
- **Onboard Serial Port1**
  Disable or enable wtih I/O address 3E8h, 3F8h as COM1 or 2E8h or 2F8h as COM2
- **Onboard Serial Port1**
  Disable or enable wtih I/O address 3E8h, 3F8h as COM1 or 2E8h or 2F8h as COM2
- **Onboard Parallel Port**
  This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. The settings are 378h, 278h, or Disabled.

Normal	The normal parallel port mode is used.
Bi-Dir	Supports bidirectional transfers on the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5 Mbs. ECP provides symmetric bidirectional communications.

- **Parallel Port DMA**
  This option is only available if the setting for the Parallel Port Mode option is ECP. The settings are Disabled, DMA CH (channel) 0, DMA CH 1, or DMA CH 3. The default setting is Disabled.

5.5 Auto-Detect Hard Disks

The Enhance IDE feature is included in all AMI BIOS. The following is a brief description of this feature.

1. Setup Changes

<I> Auto-detection

BIOS setup will display all possible modes supported by the HDD including NORMAL, LBA & LARGE. If HDD does not support LBA modes, no 'LBA' option will be shown. Users can select a mode that is appropriate for them.

<II> Standard CMOS Setup

	CYLS	Heads	Precomp	Landzone	Sector	Mode
Drive C :User(516MB)	1120	16	65535	1119	59	NORMAL
Drive D :None (203MB)	684	16	65535	685	38	----------

When HDD type is in 'user' type, the "MODE" option will be open for user to select the HDD mode.

2. HDD Modes

The Award BIOS supports 3 HDD modes: NORMAL, LBA & LARGE.

- **NORMAL mode**
  A generic access mode wherein neither the BIOS nor the IDE controller will make any transformations during accessing. The maximum number of cylinders, head & sectors for NORMAL mode are 1024, 16 & 63.

	no. Cylinder	(	1024)
x	no. Head	(	16)
x	no. Sector	(	63)
x	no. per sector	(	512)
			528 Megabytes

  If user sets his HDD to NORMAL mode, the maximum accessible HDD size will be 528MB even though its physical size may be greater than that!

- **LBA (Logical Block Addressing) mode**
  A new HDD accessing method to overcome the 528MB bottleneck. The number of cylinders, heads & sectors shown in setup may not be the number physically contained in the HDD.

  During HDD accessing, the IDE controller will transform the logical address described by sector, head & cylinder number into its own physical address inside the HDD.

  The maximum HDD size supported by LBA mode is 8.4GB which is obtained by the following formula:

	no. Cylinder	(	1024)
x	no. Head	(	255)
x	no. Sector	(	63)
x	bytes per sector	(	512)
			814 Gigabytes

- **LARGE mode**

  Extended HDD access mode supported by Award Software.

  Some IDE HDDs contain more than 1024 cylinder without LBA support (in some cases, user does not want LBA). The Award BIOS provides another alternative to support these kinds of HDD!

  Example of LARGE mode:

CYLS	HEADS	SECTOR	MODE
1120	16	59	NORMAL
560	32	59	LARGE

  BIOS tricks DOS (or other OS) that the number of cylinders is less than 1024 by dividing it by 2. At the same time, the number of heads is multiplied by 2. A reverse transformation process will be made inside INT13h in order to access the right HDD address!

  Maximum HDD size:

no. Cylinder	(	1024)
x no. Head	(	32)
x no. Sector	(	63)
x bytes per sector	(	512)
		1 Gigabytes

5.6 Change Supervisor Password

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Enter new supervisor password:
Change the supervisor password
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

5.7 Auto Configuration with Optimal Setting

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Load high performance settings (Y/N) ? N
Load configuration settings giving highest performance
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

This option allows you to load the default values to your system configuration. These default settings are optimal and enable all high performance features.

5.8 Auto Configuration with Fail Safe Setting

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Load failsafe settings (Y/N) ? N
Load failsafe configuration settings
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

This option allows you to load the troubleshooting default values permanently stored in the BIOS ROM. These default settings are non-optimal and disable all high-performance features.

5.9 Save Settings and Exit

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Save current settings and exit (Y/N) ? Y
Write the current settings to CMOS and exit
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

This option allows you to determine whether to accept the modifications or not. If you type “Y”, you will quit the setup utility and save all changes into the CMOS memory. If you type “N”, you will return to Setup utility.

5.10 Exit Without Saving

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto Detect Hard Disks
Quit without saving (Y/N) ? N
Exit without saving the current settings
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Select this option to exit the Setup utility without saving the changes you have made in this session. Typing “Y” will quit the Setup utility without saving the modifications. Typing “N” will return you to Setup utility.

This page does not contain any information.

Appendix A
Watchdog Timer

The watchdog timer uses a 32.768 KHz frequency source with a 24-bit counter. Its time range stretches from 30.5 ms to 512 sec. with a resolution of 30.5 ms. When the watchdog times out a System RESET, NMI or IRQ can be invoked. Watchdog timer control and the 24-bit counter itself occupy 6 consecutive 8-bit address locations.

When functioning properly the system resets the watchdog timer periodically to prohibit that it times out. If the watchdog timer times out, it will RESET the system, or generate and NMI or IRQ, depending on its configuration.

Watchdog or System Timer

Another great application is to generate a periodic IRQ signal. Under DOS environment, the 8254, system timer 0, will generate IRQ0 every 54.9 ms. The watchdog is like system timer 0. It can be programmed to periodically generate a configurable IRQ. It may be clear that the selected IRQ, will be no longer available to the system.

Configuring the WDT by Software

Chipset Configuration Registers

The M6117D configuration register INDEX 37H, 38H, 39H, 3AH, 3BH, 3CH are used to control the watchdog functions and/or display its current status.

Enable/Disable Watchdog - INDEX 37H

Bit	Value	Action
7	reserved	Do not modify the value of these bits!
6	0 1	Disable watchdog timer Enable watchdog timer
5-0	Other function	Do not modify the value of these bits!

Watchdog Time Out Action - INDEX 38H

Bit	Value	Action
7-4	0000	No output signal
	0001	IRQ3
	0010	IRQ4
	0011	IRQ5
	0100	IRQ6
	0101	IRQ7
	0110	IRQ9
	0111	IRQ10
	1000	IRQ11
	1001	IRQ12
	1010	IRQ14
	1011	IRQ15
	1100	NMI
	1101	System RESET
	1110	No output signal
	1111	No output signal
3-0	Other function	Do not modify the value of these bits!

Watchdog Timer - INDEX 39H, 3AH, 3BH

Index	3BH	3AH	39H
Bits	D7……D0	D7……D0	D7……D0
counter	[VSB……	……	……LSB]

For example

Index	3Bh	3AH	39H	Time out
	00h	00h	01h	30.5µs
	00h	00h	02h	61µs
	00h	01h	00h	7.8 ms
	00h	02h	00h	15.6 ms
	01h	00h	00h	2 s
	02h	00h	00h	4 s
	FFh	FFh	FFh	512 s

Timeout Status & Reset - INDEX 3CH

Bit	Value	Action
7	0 1	Timeout has not occurred Timeout has ocurred
6		
5	1 0	Reset timer Has no meaning
4-0		Other function, do not modify these bits

Programming the Watchdog

To perform any operation on the M6117D configuration registers, you always have to unlock first and lock the registers afterwards.

Unlock configuration register

```
mov al, 013h
out 22h, al
nop
nop
mov al, 0c5h
out 23h, al
nop
nop
```

Lock configuration register

```
mov al, 013h
out 22h, al
nop
nop
mov al, 000h
out 23h, al
nop
nop
```

Read the value of a configuration register

For example, read INDEX 3CH:

Unlock configuration register

```
mov al, 03ch
out 22h, al
nop
nop
in al, 23h
nop
nop
push ax
```

Lock configuration register

```
pop ax ;AL - result
```

Write data to configuration register

For example, write 0FFh to INDEX 3Bh :

Unlock configuration register

```
mov al, 03bh
out 22h, al
nop
nop
mov al, 0ffh
out 23h, al
nop
nop
```

Lock configuration register

Watchdog Program Example

We use the following sequence to initialize the watchdog timer:

Step 1. Unlock configuration register.

Step 2. Disable watchdog timer by setting INDEX 37H Bit 6 to '0'.

Step 3. Set the expected counter value to INDEX 3BH, 3AH, 39H.

Step 4. Select timeout action from INDEX 38H Bit 7-4.

Step 5. Enable watchdog timer by setting INDEX 37H Bit 6 to '1'.

Step 6. Lock configuration register.

Example: Set timeout to 128 sec to generate a system RESET.

```
; Please use MASM to compiler the following program
; Execute under DOS environment
dosseg
. model small
. stack 100h
.code
main proc
       mov ax, 0c513h ; Unlock config. register
       call writechip
       mov ax, 03737h ; Disable watchdog timer
       call readchip
       and al, 10111111b
```

```
        xchg ah, al
        call writechip
        mov ax, 0403bh ; Set the expected counter
                       ; value
        call writechip ; to [400000h]
        mov ax, 0003ah ; 30.5*sec*400000h= 128 sec
        call writechip
        mov ax, 00039h
        call writechip
        mov ax, 03838h ; Select “system reset” as
                       ; timeout action
        call readchip
        and al, 00001111b
        or al, 11010000b
        xchg ah, al
        call writechip
        mov ax, 03737h ; Enable watchdog timer
        call readchip
        or al, 01000000b
        xchg ah, al
        call writechip
        mov ax, 00013h ; Lock config. register
        call writechip
        mov ax, 04c00h
        int 21h
        main endp
readchip proc
        out 22h, al
        nop
        nop
        in al, 23h
        nop
        nop
        ret
readchip endp
writechip proc
        out 22h, al
        nop
        nop
        xchg ah, al
        out 23h, al
```

```
        nop
        nop
        xchg ah, al
        ret
writechip endp
end main
```

Reset watchdog timer

Resets the watchdog timer periodically to prevent timeout.

```
mov ax, 0c513h ; Unlock configuration
                 ; register
call writechip
mov ax, 03C3Ch ; Reset watchdog timer
                 ; counter
call readchip
or al, 00100000b ; The counter is reset at
xchg ah, al ; out 23h, al
call writechip
mov ax, 00013h ; Lock configuration
                 ; register
call writechip
```

(the above code uses readchip and writechip procedures)

Appendix B
System Assignments

System I/O Ports

The x86 CPU communicates via I/O ports. It has a total of 1KB port addresses able to be assigned to other devices via I/O expansion cards.

Address	Devices
000-01F	DMA controller #1
020-03F	Interrupt controller #1
040-05F	Timer
060-06F	Keyboard controller
070-07F	Real time clock, NMI
080-09F	DMA page register
0A0-0BF	Interrupt controller #2
0C0-0DF	DMA controller #2
0F0	Clear math co-processor busy signal
0F1	Reset math co-processor
0F8-0FF	Math processor
10C-10E	RAM/ROM disk program port address
120-123	Watch-dog timer operation
1F0-1F8	Fixed disk controller
200-207	Game port
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel port #1
3F0-3F7	Floppy disk controller
3F8-3FF	Serial port #1(COM1)
2F8-2FF	Serial port #2(COM2)
370	Onboard I/O (SMC37C669) Configuration Register

DMA Channel Assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Available
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

Interrupt Assignments

The **SBC8233 Series** is a fully PC compatible control board. It consists of 16 ISA interrupt request lines and 4 of the 16 can be either ISA or PCI. The mapping list of the 16 interrupt request lines is shown below;

NMI	Parity check error
IRQ0	System timer output
IRQ1	Keyboard
IRQ2	Interrupt rerouting from IRQ8 through IRQ15
IRQ3	Serial port #2
IRQ4	Serial port #1
IRQ5	Selectable for Parallel port
IRQ6	Floppy disk controller
IRQ7	Parallel port #1
IRQ8	Real time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 mouse
IRQ13	Math co-processor
IRQ14	Primary IDE channel
IRQ15	Reserved

1st MB Memory Map

Address	Size Description
00000000h-0009FFFFh	640K Host access map to the main memory
000A0000h-000BFFFFh	128K Video frame buffer
000C0000h-000C3FFFh	16K Reserved for Shadow VGA BIOS
000C4000h-000C7FFFh	16K Reserved for Shadow VGA BIOS
000C8000h-000CBFFFh	16K Reserved for Shadow ROM device
000CC000h-000CFFFFh	16K Reserved for Shadow ROM device
000D0000h-000DFFFFh	64K Reserved for Shadow ROM device

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Appendix C
POST Error Codes

Beep Codes

Fatal errors, which halt the boot process, are communicated through a series of audible beeps. If AMI BIOS POST can initialize the system video display, it displays the error message. Displayed error messages, in most cases, allow the system to continue to boot. Displayed error messages are described on the following table.

Beep Error Messages

Beeps	Error Message	Description
1	DRAM Refresh Failure	The memory refresh circuitry of the board is faulty.
2	Parity Circuit Failure	A parity error was detected in the base memory (first 64k Block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64k of memory.
4	System Timer Failure	Timer #1 on the system board has failed to function properly.
5	Processor Error	The CPU on the system board has generated an error.
6	Keyboard Controller 8042-Gate A20 error	The keyboard controller (8042) contains the gate A20 switch that allows the computer to operate in virtual mode. This error message means that the BIOS is not able to switch the CPU into protected mode.
7	Virtual Mode (processor) Exception error	The CPU on the motherboard has generated an Interrupt Failure exception interrupt.

Continued . . . . .

Beeps	Error Message	Description
8	Display Memory R/W Test Failure	The system video adapter is either missing or Read/Write Error its memory is faulty. This is not a fatal error.
9	ROM-BIOS Checksum Failure	The ROM checksum value does not match the value encoded in the BIOS. This is good indication that the BIOS ROMs went bad.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM has failed.
11	Cache Memory Bad — Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. *Do not press <Ctrl> <Alt> <Shift> <+> to enable cache memory.*

Other AMI BIOS POST Codes

- 2 short beeps — POST failed. This is caused by a failure of one of the hardware testing procedures.
- 1 long & 2 short beeps — Video failure. This is caused by one of two possible hardware faults. 1) Video BIOS ROM failure, checksum error encountered. 2) The video adapter installed has a horizontal retrace failure.
- 1 long & 3 short beeps — Video failure. This is caused by one of three possible hardware problems. 1) The video DAC has failed. 2) the monitor detection process has failed. 3) The video RAM has failed.
- 1 long beep — POST successful. This indicates that all hardware tests were completed without encountering errors.

Troubleshooting

If the Computer Beeps

If it beeps...	then...
1, 2, or 3 times...	re-install the memory SIMMs or DIPs. If the system still beeps, replace the memory.
No beeps, No boot	If no beeps are heard and no display is on the screen, The first thing to check is the power supply. Connect a LED to the POWER LED connection on the motherboard. If this LED lights and the drive(s) spin up then the power supply will usually be good. Next, inspect the motherboard for loose components. A loose or missing CPU, BIOS chip, Crystal Oscillator, or Chipset chip will cause the motherboard not to function. Next, eliminate the possibility of interference by a bad or improperly set up I/O card by removing all card except the video adapter. The system should at least power up and wait for a drive time-out. Insert the cards back into the system one at a time until the problem happens again. When the system does nothing, the problem will be with the last expansion card that was put in. If the above suggestions fail to cause any change in the malfunction of the system, the motherboard must be returned for repair.
6 times...	re-install the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse (if the keyboard has one).
8 times...	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times...	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times...	re-install the cache memory on the motherboard. If it still beeps, replace the cache memory.
4, 5, 6, 7, or 10 times...	the motherboard must be repaired or replaced.

Screen Error Messages

- **8042 Gate A20 Error**
  Gate A20 on the keyboard controller (8042) is not working.
- **Address Line Short!**
  Error in the address decoding circuitry.
- **Cache Memory Bad, Do Not Enable Cache!**
  Cache memory is defective.
- **CH2 Timer Error**
  There is an error in timer 2. Several systems have two timers.
- **CMOS Battery State Low**
  The battery power is getting low. It would be a good idea to replace the battery.
- **CMOS Checksum Failure**
  After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value.
- **CMOS System Options Not Set**
  The values stored in CMOS RAM are either corrupt or nonexistent.
- **CMOS Display Type Mismatch**
  The video type in CMOS RAM is not the one detected by the BIOS.
- **CMOS Memory Size Mismatch :**
  The physical amount of memory on the motherboard is different than the amount in CMOS RAM.
- **CMOS Time and Date Not Set :**
  Self evident.
- **Diskette Boot Failure**
  The boot disk in floppy drive A: is corrupt (virus?). Is an operating system present?
- **Display Switch Not Proper**
  A video switch on the motherboard must be set to either color or monochrome.
- **DMA Error**
  Error in the DMA controller.
- **DMA number 1 Error**
  Error in the first DMA channel.

- **DMA number 2 Error**
  Error in the second DMA channel.
- **FDD Controller Failure**
  The BIOS cannot communicate with the floppy disk drive controller.
- **HDD Controller Failure**
  The BIOS cannot communicate with the hard disk drive controller.
- **INTR number 1 Error**
  Interrupt channel 1 failed POST.
- **INTR number 2 Error**
  Interrupt channel 2 failed POST.
- **Keyboard Error**
  There is a timing problem with the keyboard.
- **KB/Interface Error**
  There is an error in the keyboard connector.
- **Parity Error ????**
  Parity error is in system memory at an unknown address.
- **Memory Parity Error at xxxxx**
  Memory failed at the xxxxx address.
- **I/O Card Parity Error at xxxxx**
  An expansion card failed at the xxxxx address.
- **DMA Bus Timeout**
  A device has used the bus signal for more than allocated time (around 8 microseconds).

POST Card Codes

The following codes are not displayed on the screen. They can only be viewed on the LED display of a so called POST card. The codes are listed in the same order as the according functions are executed at PC startup. If you have access to a POST Card reader, you can watch the system perform each test by the value that's displayed. If the system hangs (if there's a problem) the last value displayed will give you a good idea where and what went wrong, or what's bad on the system board.

The following tables are the checkpoint lists generated by I/O 80h port in AMI runtime compressed BIOS in order of execution.

Uncompressed Code Checkpoints

Checkpoint	Description
C2	NMI is Disabled. Power on delay starting.
C5	Power-on delay complete. Going to enable ROM. (i.e., disable Cache if any)
C6	Calculating ROM BIOS checksum.
C7	ROM BIOS checksum passed. CMOS shutdown register test to be done next.
C8	CMOS shutdown register test done. CMOS checksum calculation to be done next.
CA	CMOS checksum calculation is done, CMOS Diag byte written. CMOS status register about to init for date and time.
CB	CMOS status register init done. Any initialization before keyboard BAT to be done next.
CD	BAT command to keyboard controller is to be issued.
CE	Keyboard controller BAT result verified. Any initialization after KB controller BAT to be done next.
CF	Initialization after KB controller BAT done. Keyboard command byte to be written next.
D1	Keyboard controller command byte is written. Going to check pressing of <INS> key during power-on.
D2	Checking for pressing of <INS> key during power-on done. Going to disable DMA and Interrupt controllers.

Runtime Code is Uncompressed

Checkpoint	Description
D3	DMA controller #1, #2, interrupt controller #1, #2 disabled. Video display is disabled and port-B is initialized.
D4	Chipset initialization/ auto memory detection over. To uncompress the RUNTIME code.
D5	RUNTIME code is uncompressed.
DD	Transfer control to uncompressed code in shadow ram at F000:FFF0.
01	Processor's register test about to start, and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete. To check soft reset/power-on.
05	Soft reset/power-on determined. Going to disable Cache if any.
06	POST code to be uncompressed.
08	POST code is uncompressed. CMOS checksum calculation to be done next.
09	CMOS checksum calculation is done, CMOS Diag byte written. CMOS init to begin (If "INIT CMOS IN EVERY BOOT IS SET").
0A	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
0B	CMOS status register init done. Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller.
0D	BAT command to keyboard controller is issued. Going to verify the BAT command.
0E	Keyboard controller BAT result verified. Any initialization after KB controller BAT to be done next.
0F	Initialization after KB controller BAT done. Keyboard command byte to be written next.
10	Keyboard controller command byte is written. Going to issue Pin-23, 24 blocking/unblocking command.
11	Pin-23, 24 of keyboard controller is blocked/unblocked. Going to check pressing of <INS> key during power-on.

Continued . . . . .

Checkpoint	Description
12	Checking for pressing of <INS> key during power-on done. Going to disable DMA and interrupt controllers.
13	DMA controller #1, #2, interrupt controller #1, #2 disabled. Video display is disabled and port-B is initialized. Chipset init about to begin.
14	Chipset initialization over. 8254 timer test about to start.
19	8254 timer test over. About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
20	Memory Refresh period 30 micro second test complete. Base 64K test about to start.
23	Base 64K test passed. Going to set BIOS stack and to do any setup before Interrupt vector init.
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt Vector initialization done. Going to read input port of 9042 for turbo switch (if any) and to clear password if post diag switch is on.
26	Input port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization for turbo switch is over. Any initialization before setting Video mode to be done next.
28	Initialization before setting Video mode is complete. Going for monochrome mode and color mode setting.
2A	Different BUSes init (system, static, output devices) to start if present. (Please see Reference for details of different BUSes)
2B	About to give control for any setup required before optional Video ROM check.
2C	Processing before Video ROM control is done. About to look for optional Video ROM and give control.
2D	Optional Video ROM control is done. About to give control to do any processing after Video ROM returns control.
2E	Return from processing after the Video ROM control. If EGA/VGA not found then do display memory R/W test.

Continued . . . . .

Checkpoint	Description
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different BUSes init (input, IPL, general devices) to start if present. (Please see Reference for details of different BUSes)
39	Display different BUSes initialization error messages. (Please see Reference for details of different BUSes)
3A	New cursor position read and saved. Going to display the Hit <DEL> message.
3B	Hit <DEL> message displayed. Virtual mode memory test about to start.
40	Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the Virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640K memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.

Continued . . . . .

Checkpoint	Description
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64K memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line.
57	A20 address line disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
65	DMA #2 base register test passed. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
7F	Extended NMI sources enabling is in progress.

Continued . . . . .

Checkpoint	Description

80	Keyboard test started. Clearing output buffer, checking for stuck key. About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written, Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or by pass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message display. <WAIT...>message displayed. About to do Main and Video BIOS shadow.
8C	Main and Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Set up options are programmed, mouse check and init to be done next.
8E	Mouse check and initialization complete. Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
94	Hard disk setup complete. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support, hdisk type-47. Init of different BUSes optional ROMs from C800 to start. (Please see Reference for details of different BUSes)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.

Continued . . . . .

Checkpoint	Description

98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after co-processor test is complete. Going to check extd keyboard, keyboard ID and num-lock.
9F	Extd keyboard check is done, ID flag set, num-lock on/off, keyboard ID command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to set the keyboard typematic rate.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
B0	System configuration is displayed. Going to uncompress SETUP code for hot-key setup.

Continued . . . . .

Checkpoint	Description

B1	Uncompressing of SETUP code is complete. Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT 19h boot loader.

The following table contains all AMI BIOS beep codes. Except for Beep Code 8, they are always fatal.

Beep Code	Error Message	Description
1 beep	Refresh Failure	The memory refresh circuitry the motherboard is faulty.
2 beeps	Parity Error	A parity error was detected in the first 64KB block of memory.
3 beeps	Base 64KB Memory Failure	Memory failure in first 64KB.
4 beeps	Timer Not Operational	A memory failure occurred within the first 64KB of memory, or Timer 1 on the motherboard is not functioning.
5 beeps	Processor Error	The CPU (Central Processing Unit) on the motherboard generated an error.
6 beeps	8042-Bate A20 Failure	Gate A20 on the keyboard controller (8042) allows the CPU to operate in protected mode. The BIOS is not able to switch the CPU to protected mode.
7 beeps	Processor Exception Interrupt Error	The CPU generated an exception interrupt.
8 beeps	Display Memory Read/ Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9 beeps	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10 beeps	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM failed.
11 beeps	Cache Error/External Cache Bad	The external cache is faulty.

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